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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/909,507	07/20/2001	Gyle D. Yearsley	M-11750 US	4144

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EXAMINER	
PAN, DANIEL H	
ART UNIT	**PAPER NUMBER**
2183	7

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/909,507	YEARSLEY ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16-22* is/are allowed.

6)☒ Claim(s) *1,3-12,14 and 15, 23-25* is/are rejected.

7)☒ Claim(s) *2,13 , 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-26 are presented for examination.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1,3-5, ,8,9,11,12,14,15 are rejected under 35 U.S.C. 102(e) as being anticipated by Joy et al. (6,341,347).

3. As to claim 1, Joy disclosed a system including at least :

a) using a shared pipeline instruction datapath (see col.9, lines 1-6 [320] for the instruction data and lines 36-40 [330] for the instructions) and a shared a shared pipeline processing unit (see fig.3, [300 314]) to execute a first pipeline (thread 0] under a first context (see the processing of the current executing tread and the machine state in col.8, lines 45-58 or the active CPU with the context bit in col.13, lines 55-64);

b) receiving a request to execute under a second context (see the corresponding machine state), enabling a second pipeline to execute under a second context (see the switching to the previous thread in col.8, lines 20-25, lines 45-58, see the request to initiate the switch to another virtual CPU under updated state in col.13, lines 55-64, see also the context switching involving the saved states in col.6, lines 36-49 for background

teaching of the corresponding context, see also the stall signal for notifying the stall in col.2, lines 15-22);

c) detecting a halt (the miss which caused a stall) in execution of the first thread (see the current thread caused a stall in col.8, lines 20-25, lines 45-53);

d) using the shared datapath and shared pipeline unit (see fiog.3) to execute the second pipeline after the detection (see the previous thread or the replacing virtual CPU in col.8, lines 20-25, lines 45-58, col.13, lines 55-64, col.14, lines 17-30).

4. AS to the language of "receive a request", the source of the request is not being recited in the claim. Applicant teaches that the request is from the peripheral component (page 8, lines 14-16). However, this feature is not being recited in the claim. Nevertheless, Joy disclosed that in some context switches which are typically made with response to interrupts, including software and hardware interrupt , both internal and external, of a processor (e.g. see col.14, lines 62-67). From the above teaching , it is clear that the interrupts from external devices, such as a peripheral device, were also applicable in Joy, and that the interrupts, either software or the hardware, in order to have the response, they must be in the form of requests. Applicant is welcome to provide feedback in the next response.

5. As to claims 3, 5, Joy also included a thread end because it was also directed to prioritizing the thread (see col.2, lines 25-28, col.16, lines 21-28 ; the higher priority has to be finished before the lower priority).

6. As to claim 4, Joy was also directed to access stall (e.g. see the cache miss stall in col.8, lines 45-47).

7. As to claim 8, Joy taught a context switching to another thread (the second pipeline) based on lacking system (e.g. see col.16, 29-37). Therefore, if the locking is enabling , the context switching should be permitted.

8. As to claim 9, Joy also included :

a) detecting a halt (context switch caused by stall, priority, interrupt etc , see col.2, lines 10-32) of second pipeline (see replacing thread or CPU in col.8, lines 45-58, col.14, lines 17-31, see col.7, lines 40-45) ;

b) and resume of the second pipeline (see the resume of the stalling or the replacing thread or CPU in col.8, lines 45-58, col.14, lines 17-31, see col.7, lines 40-45) .

As to claim 11,14, Joy disclosed a shared pipeline instruction path (see fig.3 shared instruction data cache and instruction cache);

b) a shared pipeline processing unit (see gif.3 300 314);

c) a first set of pipeline registers [flip-flops] (see fig.4B 430);

d) a second storage cells (440);

e) control multiplexer [multiplexer or switch] coupled to the first pipeline register and second register to the shared datapath and share pipelined processing unit (e.g. see additional storage cells used and the multiplexer in col.11, lines 48-67, see fig.3 for the shared pipelining processing 314 and shared datapath 330 320);

f) execution stage (e.g. see col.3, lines 16-25 for the execution of the pipeline threads).

As to claim 15, Joy also included a memory controller (e.g. see col.9, lines 36-46 {IMMU] , col.22, lines 40-43 [MCU]),

9. As to claim 12, Joy also included a pipeline controller (see the control block and storage in fig.4A for controlling the pipeline registers , col.10, lines 23-32, lines 37-40).

10.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claim 23 is rejected under 35 U.S.C. 102 (a) and (b) as being (anticipated) by Golson (5,390,332).

12. As to claim 23, Golson disclosed a communication system (see the network in fig,1) comprising at least ;

a) a communication engine [200 240] comprising a pipeline (concurrent) context switch microprocessor [200] (e.g. see the microprocessor 200 was a multitasking and can execute multiple processes concurrently in col.7, lines 22-24, see also the execution of

the next process and the resume of the current process col.7, lines 60-68, col.8, lines 1-8);

b) a system block [100][120][130][140] comprising a system processor [SPARC 100] coupled to the communication engine (e.g. see fig.3).

Golson did not explicitly show his system processor [Host 100 or the SPARC 100, see fig.3] was a microprocessor as claimed. However, Golson , in the same patent , disclosed that his system processor 100 [host 100] was a UNIX based processor manufactured by Sun Microsystems (col.3,lines 55-62), and that the host processor 100 was a SPARC workstation (col.4, lines 42-51). It should not be difficult to see that the system processor 100 SPARC of Golson should have a built-in microprocessor therein in order to achieve the multitasking processing (see the multitasking, multiwindows in col.7, lines 14-22) for the host process , and it should have been unusual for a workstation or a host not to have a microprocessor. IN other words, has applicant seen any workstation which performs multiprocessing and does not have a microprocessor ? Therefore, for the above reasons, the claimed invention is found anticipated by Golson. Applicant is welcome to provide feedback in the next response. Since the microprocessor is not clearly shown in Golson in the system processor [SPARC 100], alternative interpretation under the obviousness rejection will follow in this action.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 6,7,10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joy (6,341,347) in view of Swoboda et al. (6,553,513).

14. As to claims 6, 7, limitations of the parent claim have been discussed in paragraph # 3 , therefore, it will not be repeated herein. Joy did not specifically show flush of the instructions as claimed. However, Swoboda disclosed a system for flushing the instructions (e.g. see col.18, lines 8-10). It would have been obvious to one of ordinary skill in the art to use Swoboda in Joy flushing the instructions as claimed because the use of Swoboda could provide the processing ability of Joy to increase the execution bandwidth of the multiple threads without extra cycle, and therefore, a minimized the latency caused by unwanted instructions, and it could be readily achieved by predefining flush condition of Swoboda into the configuration of Joy with modified control parameters, such as the command or enabling signal of flush, so that Swoboda's instruction flush could be recognized by Joy, and one of ordinary skill in the art should be able to recognize that Swoboda could be used for providing solution to the desirability of reducing the wasted cycle due to the stalling and increasing the proportion of the execution time in Joy (see Joy's col.2, lines 38-45), and for the above reasons provided a motivation .

15. As to claim 10, Joy did not specifically show the debug context as claimed. However, Swoboda included a debug context (e.g. see col.14, lines 44-62). It would have been obvious to one of ordinary skill in the art to use Swoboda in Joy for including the debug context as claimed because the use of Swoboda could provide Joy the control capability to adapt to specific level of processing, such as the restore period, and preserved the processing conditions or states as needed, and Joy also taught the resume of the previously postponed pipelined thread (e.g. see col.8, lines 56-58) which was a suggestion of the applicability of a debug context (e.g. through the use of restoration of status registers etc) in order to resume the previous processing , and in doing so, provided a motivation.

16. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Golson (5,390,332) in view of Bunnell et al. (5,594,903) .

17. As to claim 23, Golson disclosed a communication system (see the network in fig,1) comprising at least ;

a) a communication engine [200 240] comprising a pipeline (concurrent) context switch microprocessor [200] (e.g. see the microprocessor 200 was a multitasking and can execute multiple processes concurrently in col.7, lines 22-24, see also the execution of the next process and the resume of the current process col.7, lines 60-68, col.8, lines 1-8);

b) a system block [100][120][130][140] comprising a system processor [SPARC 100] coupled to the communication engine (e.g. see fig.3).

18. Golson did not explicitly show his system processor [Host 100 or the SPARC 100, see fig.3] was a microprocessor as claimed. However, Golson , in the same patent , disclosed that his system processor 100 [host 100] was a UNIX based processor manufactured by Sun Microsystems (col.3,lines 55-62), and that the host processor 100 was a SPARC workstation (col.4, lines 42-51). It would have been obvious to one o ordinary skill in the art to recognize that the system processor 100 SPARC of Golson should have a built-in microprocessor therein in order to achieve the multitasking processing (see the multitasking, multiwindows in col.7, lines 14-22) for the host process. Nevertheless, since the microprocessor was not being shown the workstation (the host 100) in Golson, Bunnell , a secondary reference, is being used to show that a workstation , such as SPARC, had a SAPRC microprocessor. Therefore, Bunnell disclosed a system including a SAPRC microprocessor used for work stations (e.g. see col.4, lines 26-40). It would have been obvious to one of ordinary skill in the art to use Bunnell in Golson for including the microprocessor into the system processor (SPARC 100) of Golson because the use of Bunnell could provide control of the host processor 100 of Golson to adapt to more complex processing based on a specific architectural requirements of the microprocessor, such as the word width and the format for adapt to the multitasking processing, and for the above reasons , provided a motivation.

19. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Golson (5,390,332) in view of Bunnell et al. (5,594,903) as applied to claim 23 above, and further in view of Diepstraten et al. (6,205,468).

20. As to claim 24, neither Golson nor Bunnell specifically teach the single integrated circuit as claimed. However, Diepstraten disclosed a context microprocessor developed for a single integrated circuit (e.g. see col.3, lines 15-19). It would have been obvious to one of ordinary skill in the art to use Diepstraten in Golson for including single integrated circuit as claimed because the use of Diepstraten could reduce the hardware overheads and therefore, the cost, of Golson by the integration of circuit components of Golson into a single package with the predefined context switching configuration parameters of Diepstraten , developed and applicable in single chip microprocessors, recognizable by Golson, and therefore, provided a motivation.

21. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Golson (5,390,332) in view of Bunnell et al. (5,594,903) as applied to claim 23 above, and further in view of Joy (6,341,347).

22. As to claim 25, both Golson and Bunnell disclosed a multiplexer (the context switching). But, neither Golson nor Bunnell disclosed :

a) the a shared pipeline processing unit;

b) a first set of pipeline registers;

c) a second pipeline registers (440);

d) the control multiplexer coupled to the shared datapath and processing pipeline unit and the pipeline registers .

However, Joy disclosed at least :

a) a shared pipeline processing unit (see gif.3 300 314);

b) a first set of pipeline registers [flip-flops] (see fig.4B 430);

c) a second pipeline registers (storage cells 440);

d) control multiplexer [multiplexer or switch] coupled to the first pipeline register and second register to the shared datapath and share pipelined processing unit (e.g. see additional storage cells used and the multiplexer in col.11, lines 48-67, see fig.3 for the shared pipelining processing 314 and shared datapath 330 320);

23. It would have been obvious to one of ordinary skill in the art to use Joy in Golson for including the shared pipeline unit and the shared datapath with the multiplexer as claimed because the use of Joy could provide the greater processing structure of Golson to accept different type of interface connection such as the common or shared data bus, thereby minimizing the circuit overheads of the system connection, and it could be done by introducing the circuit connection of Joy into Golson's configuration file with adjustable bit format and control variables (read/write commands) so the shared pipeline and datapath could be recognized by Golson to achieve the shared bus structure, and for the above reasons , provided a motivation.

24. Claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the

base claim and any intervening claims. None of the prior art of record further teaches the stalling for a clock cycle and used the clock cycle to fetch address vector of eh second pipeline.

25. Claim 13 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the shared instruction datapath comprises a pipeline address stage, pipeline fetch stage, a pipeline memory stage, and pipeline decode stage.

26. Claims 16-22 are allowable over the art of record for further reciting the combined features of the first set of processing registers and the second set of processing registers and the set of shared registers associated both the first context and second context, and the first context register and the second context register.

27. Claim 26 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the combined features of the shared instruction datapath, the first set of processing registers and the second set of processing registers and the set of shared registers associated both the first context and second context, and the first context register and the second context register.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a). Riches, Jr. et al. (5,490,265) is cited for the basic teaching of the halting of the pipeline (e.g. see col.4, lines 45-56)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

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